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10/714,674	11/18/2003	Rebecca E. Hebda	02207/17415	2323

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EXAMINER	
JOHNSON, BRIAN P	
ART UNIT	PAPER NUMBER
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/714,674	HEBDA ET AL.	
	Examiner	Art Unit	
	Brian P. Johnson	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-21 and 23-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21 and 23-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 1-21, 23-42 have been examined.

Acknowledgment of papers filed: amendments and remarks filed 18 October 2006. The papers filed have been placed on record.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 21 and 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, the term "quick access" is indefinite.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3-9, 11-19, 21, 23-31, 33-35, and 37-41 are rejected under 35 U.S.C. 103(a) as being 35 U.S.C. 103(a) as being unpatentable over Carbine (U.S. Patent No. 5,630,083) in view of Kipp (U.S. Patent No. 5,765,220).

6. Regarding claim 1, Carbine discloses a processor comprising: a plurality of programmable logic arrays (PLAs) (col 2 lines 37-45);

Note that, within the processing system, all components are considered to be "coupled". Consequently, any limitation regarding the coupling of two components are appropriately anticipated by the references on record.

An instruction pointer sequencing logic/predictor component (fig 5 reference 534 and col 11 lines 24-30) coupled to said instruction queue; a micro-operation memory (col 11 lines 1-4); coupled to a micro-instruction cache (col 11 lines 1-4)

Note that according to the American Heritage Dictionary, a cache is defined as "an area of computer memory devoted to high-speed retrieval of frequently used or requested data." So, in this case, the UOP ROM is considered to be cache.

and a trace pipe (TPIPE) (col 6 lines 14-16)

Note that paragraph 18 of the specification states, "in accordance with the embodiment of the present invention, micro-operation cache 160 may output the micro-operations to a trace pipe ("TPIPE") 190 where the micro-operations for a given instruction may be assembled into an instruction trace, if necessary, to be forwarded for execution." Accordingly, the trace pipe, as claimed, is reasonably anticipated by a typical instruction sequencer for out-of-order processors, which creates an instruction trace for execution; an element that must exist in a processor with out-of-order capabilities, as disclosed.

Coupled to said micro-operation cache and said instruction pointer queue.

Carbine fails to disclose an instruction pointer queue, rather than an instruction queue itself.

Kipp discloses the use of a cache (col 2 lines 54-56) that holds the instructions, while a pointer (index) value is contained in the instruction queue to retrieve the instruction for execution (col 5 lines 41-46).

Carbine would be motivated to utilize the pointer value contained in the instruction queue method to minimize queue storage space (and, likely, power) as described in Kipp col 5 lines 50-55, "Since the instruction address for the instructions in each cache line is stored in the instruction address only once for all eight instructions contained in a cache line, the amount of storage needed to store instruction addresses is reduced almost by a factor of eight."

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the computing system of Carbine, and include the pointer queue method as disclosed by Kipp, rather than a typical instruction queue/buffer.

7. Regarding claim 3, Carbine/Kipp discloses the processor of claim 1 wherein said plurality of PLAs are coupled to an alias logic component (col 5 line 32).

8. Regarding claim 4, Carbine/Kipp discloses the processor of claim 1 wherein said instruction pointer queue is to store said instruction pointer for said first micro-operation in each instruction (col 2 llines 57-63).

9. Regarding claim 5, Carbine/Kipp discloses the processor of claim 3 wherein said instruction pointer queue is at least three micro-instruction pointers wide (col 6 lines 7-9).

Note that since Carbine alone contains a three-wide instruction queue, the instruction pointer queue after the combination would be expected to have the same width.

10. Regarding claim 6, Carbine/Kipp discloses the processor of claim 1 wherein said instruction pointer sequencing logic/predictor component comprises: a four-to-one multiplexer (fig 5 reference 560) to receive a micro-instruction pointer from a PLA and output a micro-instruction pointer for a next micro-operation (fig 5);

Note that, clearly, after the Carbine/Kipp combination is made, a pointer would be received by the multiplexer.

A micro-instruction pointer predictor coupled to said four-to-one multiplexer (fig 5 reference 534), said micro-instruction pointer predictor to output a predicted next micro-instruction pointer to said multiplexer (col 11 lines 24-30); and an incrementer component coupled to said four-to-one multiplexer, said incrementer component to output an incremental next micro-instruction pointer to said multiplexer (see below).

Note that the the instruction pointer queue in Kipp is considered to be an incrementer component in the sense that it outputs and incremental next microinstruction pointer to, what would be after the combination, the multiplexer.

11. Regarding claim 7, Carbine/Kipp discloses the processor of claim 6 wherein said four-to-one multiplexer is further to receive a next micro-instruction pointer from said micro-operation read only memory (col 11 lines 1-4).

12. Regarding claim 8, Carbine/Kipp discloses the processor of claim 1 wherein said micro-operation cache comprises: an at least 3-wide micro-operation cache to store commonly used micro-operations (Kipp col 5 lines 41-46).

13. Regarding claim 9, Carbine/Kipp discloses the processor of claim 1 wherein said micro-operation memory comprises: an at least 3-wide micro-operation read only memory to store all micro-operations that can be decoded from an instruction set (col 11 lines 1-4).

14. Regarding claim 11, Carbine/Kipp discloses a processor comprising: a plurality of programmable logic arrays (PLAs) (col 2 lines 37-45) to output a first instruction pointer for a first micro-instruction operation in each instruction (Kipp col 2 lines 57-63);

Note that, logically, the decoding PLA would route the index value with this combination.

An instruction pointer queue to receive the first instruction pointers (col 2 lines 57-63); an instruction pointer sequencing logic/predictor component (fig 5 reference 534 and col 11 lines 24-30)

Note that the instruction queue with the offset value can be considered a prediction circuit as well. The American Heritage College Dictionary defines a prediction as "to state or tell about, or make known in advance especially on the basis of special knowledge". The offset value, therefore, predicts the next instruction pointer (if an instruction is interpreted to be a line of the cache).

To predict a next instruction pointer for each instruction; a micro-operation cache (Kipp col 2 lines 54-56) to store a plurality of frequently used micro-instruction operations; a micro-operation memory (col 11 lines 1-4) to store a plurality of micro-instruction operations; and a trace pipe (TPIPE) to build a trace of micro-instruction operations for each instruction (col 6 lines 14-16).

Note: see claim 1.

15. Regarding claim 12, Carbine/Kipp discloses the processor of claim 11 wherein each of said plurality of PLAs to receive input from a build pipe (fig 8 reference 810).

16. Regarding claim 13, Carbine/Kipp discloses the processor of claim 11 wherein each of said plurality of PLAs receive input from an alias logic component (fig 5 references 502 and 504 input into 530, 510, 512, 514, and 516).

Note that the opcodes of the macroinstruction is considered to be an alias of the instruction; therefore, the components giving input to the PLAs shown in fig 5 are considered to be alias logic components.

17. Regarding claim 14, Carbine/Kipp discloses the processor of claim 11 wherein said instruction pointer queue is to store said instruction pointer for said first micro-operation in each instruction (col 5 lines 41-46).

18. Regarding claim 15, Carbine/Kipp discloses the processor of claim 14 wherein said instruction pointer queue is to concurrently provide up to three micro-instruction pointers (col 6 lines 7-9).

19. Regarding claim 16, Carbine/Kipp discloses the processor of claim 11 wherein said instruction pointer sequencing logic/predictor component comprises: a four-to-one multiplexer (fig 5 reference 560) to receive a micro-instruction pointer from a PLA and output a micro-instruction pointer for a next micro-operation (fig 5);

Note that, clearly, after the Carbine/Kipp combination is made, a pointer would be received by the multiplexer.

A micro-instruction pointer predictor to output a predicted next micro-instruction pointer to said multiplexer (fig 5 reference 534); and an incrementer component to output an incremental next micro-instruction pointer to said multiplexer (col 11 lines 24-30).

20. Regarding claim 17, Carbine/Kipp discloses the processor of claim 16 wherein said four-to-one multiplexer is further to receive a next micro-instruction pointer from said micro-operation read only memory (col 11 lines 1-4).

21. Regarding claim 18, Carbine/Kipp discloses the processor of claim 11 wherein said micro-operation cache is to store at least 3 micro-operations per set of commonly used micro-operations (Kipp col 5 lines 41-46).

22. Regarding claim 19, Carbine/Kipp discloses the processor of claim 11 wherein said micro-operation read only memory is store at least 3 micro-operations per set of all micro-operations that can be decoded from an instruction set (col 11 lines 1-4).

23. Regarding claims 21 and 26, Carbine/Kipp discloses a method comprising:

Storing in a cache a plurality of commonly used micro-operations for quick access (col 11 lines 1-4);

Storing a plurality of micro-operatings including said plurality of commonly used micro-operations fig 7 reference 734;

determining a first instruction pointer for a first operation in an instruction (Kipp col 4 lines 1-9);

Note that according to the American Heritage College Dictionary, the computer science definition of an instruction is "a sequence of bits that tells a computer to perform a particular operation". In light of Applicant's use of the word, an instruction can reasonably contain a variety of operations, rather than just one. Consequently, a line of cache can reasonably be considered an instruction, seeing how it is precisely a

reordered group of microinstructions that tell a computer to perform a particular operation.

Storing the first instruction pointer (Kipp col 2 lines 57-63); predicting a next instruction pointer for each additional operation in the instruction (Kipp col 2 lines 57-63);

Note that the offset value is used to predict each subsequent operation in the cache line instruction.

Reading one or more operations in the instruction using the first instruction pointer (Kipp col 3 lines 1-8) and any predicted next instruction pointers (Kipp col 3 lines 1-8); and building a trace of micro-operations using the one or more operations for the instruction (col 6 lines 14-16).

24. Regarding claim 27, Carbine/Kipp discloses the method of claims 21 and 26 further comprising: storing a plurality of commonly used operations for quick access; and storing a plurality of micro-operations including said plurality of commonly used micro-operations (Kipp col 5 lines 41-46).

25. Regarding claims 23 and 28, Carbine/Kipp discloses the method of claims 21 and 26 wherein determining a first instruction pointer for a first operation in an instruction comprises: determining the first instruction pointer for the first operation in the instruction in a programmable logic array (col 2 lines 37-45).

Note that the PLAs, which are used in part as decoders in the referenced invention, clearly must determine which operation is the first in an instruction in order to correctly route the information down the pipeline.

26. Regarding claims 24 and 29, Carbine/Kipp discloses the method of claims 22 and 27 wherein predicting a next instruction pointer for each additional operation in the instruction comprises: predicting the next instruction pointer for each additional operation in the instruction in a predictor separate from the programmable logic array (Kipp col 5 lines 41-46).

Note that the concatination of the index and offset value, used to predict the next instruction pointer, occurs outside of the PLA devices.

27. Regarding claims 25 and 30, Carbine/Kipp discloses the method of claims 24 and 29 wherein reading one or more operations in the instruction using the first instruction pointer and any predicted next instruction pointers comprises (Kipp col 2 lines 57-63): reading the one or more operations in the instruction using the first instruction pointer and any predicted next instruction pointers from a cache memory (Kipp col 5 lines 41-46) or a read only memory (col 11 lines 1-4), if the one or more operations are not in the cache memory (see below).

Note that in the referenced combination, there is no circumstance in which the operations are not in cache memory. Consequently, the fact remains true that "if the

one or more operations are not in the cache memory, the instruction pointers are read from ROM."

28. Regarding claim 31, Carbine/Kipp discloses a computer system comprising: a memory to provide program instructions (col 4 lines 59-62); and a processor coupled to said memory (col 3 lines 54-56), said processor comprising: a plurality of programmable logic arrays (PLAs) (col 2 lines 37-45); an instruction pointer queue coupled to said plurality of PLAs (Kipp col); an instruction pointer sequencing logic/predictor component (fig 5 reference 534 and col 11 lines 24-30) coupled to said instruction pointer queue; a micro-operation cache (Kipp col 2 lines 54-56) coupled to said instruction pointer sequencing logic/predictor component; a micro-operation memory (col 11 lines 1-4) coupled to said micro-operation cache; and a trace pipe (TPIPE) (col 6 lines 14-16) coupled to said micro-operation cache and said instruction pointer queue.

29. Regarding claim 33, Carbine/Kipp discloses the processor of claim 31 wherein said plurality of PLAs are coupled to an alias logic component (col 5 line 32).

30. Regarding claim 34, Carbine/Kipp discloses the processor of claim 31 wherein said instruction pointer queue is to store said instruction pointer for said first micro-operation in each instruction (col 2 llines 57-63).

31. Regarding claim 35, Carbine/Kipp discloses the processor of claim 31 wherein said instruction pointer sequencing logic/predictor component comprises: a four-to-one multiplexer (fig 5 reference 560) to receive a micro-instruction pointer from a PLA and output a micro-instruction pointer for a next micro-operation (fig 5); a micro-instruction pointer predictor (fig 5 reference 534 or Kipp col 2 lines 57-63 see claim 11) coupled to said four-to-one multiplexer, said micro-instruction pointer predictor to output a predicted next micro-instruction pointer to said multiplexer (fig 5 and Kipps col 5 lines 41-46); and an incrementer component coupled to said four-to-one multiplexer, said incrementer component to output an incremental next micro-instruction pointer to said multiplexer (see claim 6).

32. Regarding claim 37, Carbine/Kipp discloses a computer system comprising: a memory (col 4 lines 59-62) to provide program instructions; and a processor coupled to said memory (col 3 lines 54-56), said processor comprising: a plurality of programmable logic arrays (PLAs) (col 2 lines 37-45) to output a first instruction pointer for a first micro-instruction operation in each instruction (Kipp col 2 lines 57-63); an instruction pointer queue to receive the first instruction pointers (Kipp lines 57-63); an instruction pointer sequencing logic/predictor component to predict a next instruction pointer for each instruction (fig 5 reference 534 and col 11 lines 24-30); a micro-operation cache (Kipp col 2 lines 54-56) to store a plurality of frequently used micro-instruction operations; a micro-operation memory (col 11 lines 1-4) to store a plurality of micro-instruction

operations; and a trace pipe (TPIPE) (col 6 lines 14-16) to build a trace of micro-instruction operations for each instruction (see claim 1)..

33. Regarding claim 38, Carbine/Kipp discloses the processor of claim 37 wherein each of said plurality of PLAs to receive input from a build pipe that is coupled to said memory (fig 8 reference 810).

34. Regarding claim 39, Carbine/Kipp discloses the processor of claim 37 wherein each of said plurality of PLAs receive input from an alias logic component (col 5 line 32).

35. Regarding claim 40, Carbine/Kipp discloses the processor of claim 37 wherein said instruction pointer queue is to store said instruction pointer for said first micro-operation in each instruction (col 2 llines 57-63).

36. Regarding claim 41, Carbine/Kipp discloses the processor of claim 37 wherein said instruction pointer sequencing logic/predictor component comprises: a four-to-one multiplexer (fig 5 reference 560) to receive a micro-instruction pointer from a PLA and output a micro-instruction pointer for a next micro-operation (fig 5); a micro-instruction pointer predictor (fig 5 reference 534 or Kipp col 2 lines 57-63 see claim 11) to output a predicted next micro-instruction pointer to said multiplexer; and an incrementer component to output an incremental next micro-instruction pointer to said multiplexer (fig 5 and Kipps col 5 lines 41-46).

37. Claims 10, 20, 36 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carbine/Kipp in view of common art.

Regarding claims 10, 20, 36 and 42, Carbine/Kipp discloses the method and apparatus of the claims on which claims 10, 20, 36 and 42 are dependent in addition to storing micro-operations to be read in parallel with said micro-operation read only memory (col 11 lines 1-4).

Carbine/Kipp fails to disclose the use of a patch cache to store micro-operations and to be read in parallel with said micro-operation read only memory.

Applicant asserts the use of an L2 cache is common practice, and would be capable of being utilized simultaneously (in parallel with) the micro-operation read only memory.

Note that the "patch cache" is not a term that one of ordinary skill would have known. Additionally, the term in light of Applicant's specification in paragraph 17 seems to be adequately anticipated by a typical L2 cache.

Examiner asserts that the use of an L2 cache has been found to show remarkable performance gains over a single level cache.

It would have been obvious at the time of the invention for one of ordinary skill in the art to allow the micro and/or macro-instruction caches of Carbine/Kipp to be implemented with a second level cache, as in typical prior art.

Allowable Subject Matter

38. Claims 2 and 32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claims 2 and 32, no prior art on record discloses a PLA predicting the number if micro-operations in an instruction in addition to all other limitations.

Response to Arguments

39. Applicant's arguments filed 18 October 2006 have been fully considered but they are not persuasive.

40. Applicant contends that Carbine does not disclose a cache as claimed. Examiner has addressed this concern within the rejection to make it more clear.

Conclusion

41. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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